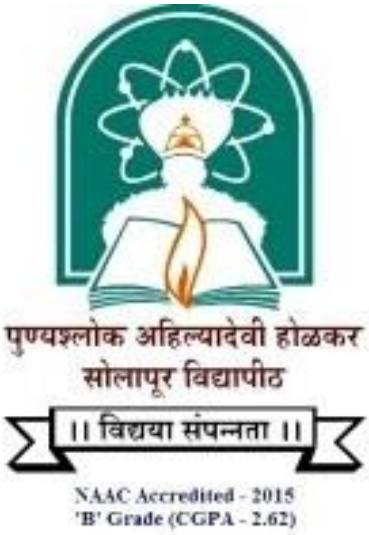

Punyashlok Ahilyadevi Holkar Solapur University, Solapur

FACULTY OF ENGINEERING & TECHNOLOGY

ELECTRONICS ENGINEERING

CBCS Syllabus for

First and Second Year M. Tech.
w.e.f. Academic Year 2023-24

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR
FACULTY OF ENGINEERING & TECHNOLOGY

STRUCTURE OF M. Tech. (ELECTRONICS ENGINEERING)
Four Semester Course

Choice Based Credit System Syllabus w.e.f. 2023 -24

Semester-I

Sr. No.	*Subject*	*Teaching Scheme*				*Credits*				*Evaluation Scheme*				
		L	*T*	*P*	*Total*	*Credits (L)*	*Credits (T)*	*Credits (P)*	*Total Credits*	*Scheme*	*Theory Marks*	*ICA- P Marks*	*ICA-T Marks*	*Total Marks*
1	Digital Design and Verification	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
2	Advanced Digital Signal Processing	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
3	Voice and Data Networks	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
4	Machine Learning©	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
5	Elective I	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
6	Seminar- I	-	-	2	2	-	-	2.0	2.0	ISE	--	50	--	50
										ESE	--	--	--	
Total		**15**	**2**	**8**	**25**	**15.0**	**2.0**	**5.0**	**22.0**		**500**	**125**	**50**	**675**

Note : *L- Lectures, P-Practical, T-Tutorial, ISE- InSemester Evaluation, ESE- End Semester Evaluation, ICA- Internal Continuous Assessment*

© - This Course is common for M.Tech. (Electronics Engineering) and M.Tech. (Computer Science & Engineering)

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR
FACULTY OF ENGINEERING & TECHNOLOGY

STRUCTURE OF M. Tech. (ELECTRONICS ENGINEERING)
Four Semester Course
Choice Based Credit System Syllabus w. e. f. 2023-24
Semester-II

Sr. No.	*Subject*	*Teaching Scheme*				*Credits*				*Evaluation Scheme*				
		L	*T*	*P*	*Total*	*Credits (L)*	*Credits (T)*	*Credits (P)*	*Total Credits*	*Scheme*	*Theory Marks*	*ICA- P Marks*	*ICA-T Marks*	*Total Marks*
1	Research Methodology & IPR©	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
2	Communication Buses & Interfaces	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
3	Advanced IOT	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
4	PLC, SCADA and Distributed Control Systems	3	-	2	5	3.0	-	1.0	4.0	ISE	30	25	--	125
										ESE	70	--	--	
5	Elective – II	3	1	-	4	3.0	1.0	-	4.0	ISE	30	--	25	125
										ESE	70	--	--	
6	Seminar- II	-	-	2	2	-	-	2.0	2.0	ISE	--	50	--	50
										ESE	--	--	--	
Total		**15**	**2**	**8**	**25**	**15.0**	**2.0**	**5.0**	**22.0**		**500**	**125**	**50**	**675**

Note : *L- Lectures, P-Practical, T-Tutorial, ISE- InSemester Evaluation, ESE- End Semester Evaluation, ICA- Internal Continuous Assessment*
© - This Course is common for M.Tech. (Electronics Engineering) and. M.Tech. (Computer Science & Engineering)

- Seminar I shall be delivered on a topic related to student's broad area of interest for dissertation work selected in consultation with the advisor after compiling the information from the latest literature. Student shall deliver seminar using modern presentation tools. A hard copy of the report (as per format specified by the department) shall be submitted to the Department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any.

- Seminar II shall be delivered on a topic related to student's particular area of interest for dissertation work selected in consultation with the advisor after compiling the information from the latest literature. Student shall deliver seminar using modern presentation tools. A hard copy of the report (as per format specified by the department) shall be submitted to the Department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any.

- **List of elective courses for semester I and II -**

Sr.	***Elective - I***	***Elective – II***
1	Wireless Sensor Networks	Mobile Technology
2	Analog & Digital CMOS VLSI Design	Real Time Systems
3	Image and Video Processing	VLSI in Signal Processing

- Courses may be added in the list of Elective I and II as and when required

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

FACULTY OF ENGINEERING & TECHNOLOGY

STRUCT RE OF M.TECH. (ELECTRONICS ENGINEERING)

Four Semester Course

Choice-Based Credit System Syllabus

Semester-III

Sr. No.	*Subject*	*Teaching Scheme*		*Credits*			*Evaluation Scheme*			
		L	*P*	*Credits (L)*	*Credits (P)*	*Total Credits*	*Scheme*	*Theory Marks*	*ICA Marks*	*Total Marks*
1	Self Learning Course	$	-	3.0	-	3.0	ISE	30	--	100
							ESE	70		
2	Open Elective Course#	3		3.0		3.0	ISE	30		100
							ESE	70		
3	Dissertation Phase I : Synopsis Submission Seminar*		@4		3.0	3.0	ISE	--	100	100
							ESE	--	--	
4	Dissertation Phase II : ICA*		-		3.0	3.0	ISE	--	100	100
							ESE	--	--	
5	Dissertation Phase II Progress Seminar*		-		3.0	3.0	ISE	--		100
							ESE	--	100	
Total		**3**	**4**	**6.0**	**9.0**	**15.0**		**200**	**300**	**500**

L- Lectures, P-Practical, T-Tutorial, ISE- In Semester Evaluation, ESE- End Semester Evaluation, ICA- Internal Continuous Assessment

Note -

- $- Being a Self Learning Course, student shall prepare for examination as per specified syllabus
- *- For all activities related to dissertation Phase I (synopsis submission seminar and progress seminar) student must interact regularly every week with the advisor.
- # - This course is common for all branches of Technology (ie for all M.Tech. Programs)

- Synopsis submission seminar shall cover detailed synopsis of the proposed work. Student shall submit synopsis of the dissertation work only after delivering this seminar.
- Progress seminar shall be delivered capturing details of the work done by student for dissertation
- Student shall deliver all seminars using modern presentation tools. A hard copy of the report shall be submitted to the department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any
- @ Indicates contact hours of students for interaction with advisor.
- Details of modes of assessment of seminar and dissertation shall be as specified in 7(III) of PG Engineering Ordinance of Solapur University, Solapur

List Self Learning Courses -

Sr.	***Self-Learning Subject***
1	Network and Internet Security
2	Programmable System on Chip (PSoC)
3	Advanced Process Control

List of Open Elective Courses-

Sr.	***Self-Learning Subject***
1	Business Analytics
2	Operation Research
3	Cost Management of Engineering Projects
4	Product Design and Development

- New Self Learning Courses and New Open Elective Courses may be added as and when required

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

FACULTY OF ENGINEERING & TECHNOLOGY
STRUCTURE OF M.E. (ELECTRONICS ENGINEERING)
Four Semester Course
Choice Based Credit System Syllabus
Semester-IV

Sr. No.	*Subject*	*Teaching Scheme*			*Credits*			*Evaluation Scheme*		
		L	*P*	*Total*	*Credits (L)*	*Credits (P)*	*Total Credits*	*Scheme*	*ICA Marks*	*Total Marks*
1	Dissertation Phase III : Progress Seminar #	-	4@	4	-	3.0	3.0	ISE	100	100
2	Dissertation Phase IV: #	-	2@	2	-	6.0	6.0	--	200	200
3	Final Submission of the Dissertation and Viva –Voce	-	-	-	-	6.0	6.0	ESE	200	200
	Total	**-**	**-**	**6**	**--**	**15.0**	**15.0**	**-**	**500**	**500**

Note –

- #- For all activities related to dissertation Phase III & IV student must interact regularly every week with the advisor.
- Progress seminar shall be delivered capturing details of the work done by student for dissertation
- Student shall deliver all seminars using modern presentation tools. A hard copy of the report shall be submitted to the Department before delivering the seminar. A PDF copy of the report must be submitted to the advisor along with other details if any.
- Student must submit a hard copy of Project Report to the department
- @ indicates contact hours of the student for interaction with the advisor
- Details of modes of assessment of seminar and dissertation shall be as specified in 7 (III) of PG Engineering Ordinance of Solapur University, Solapur.

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M. Tech. (Electronics) Semester-I

DIGITAL DESIGN AND VERIFICATION

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Practical –2Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Revision of Basic Digital Systems **(6 Hrs)**

Combinational circuits, sequential circuits, logic families, synchronous FSM and asynchronous design, metastability, clock distribution and issues, basic building blocks like PWM module, pre-fetch unit, programmable counter, FIFO, Booth's multiplier, ALU, barrel shifter etc.

Unit 2: Verilog / VHDL (7 Hrs)

Verilog/VHDL comparisons and guidelines, Verilog: HDL fundamentals, simulation, and testbench design, examples of Verilog codes for combinational and sequential logic, Verilog AMS

Unit 3: System Verilog and Verification: **(8 Hrs)**

Verification guidelines, data types, procedural statements and routines, connecting the test bench and design, assertions, basic OOP concepts, randomization, introduction to basic scripting language: Perl, Tcl/Tk

SECTION II

Unit 4: Current Challenges in Physical Design: **(8 Hrs)**

Roots of challenges, delays: wire load models generic PD flow, challenges in PD flow at different steps, SI challenge - noise & crosstalk, IR drop, Process effects: proc ss antenna effect & electro migration

Unit 5: Programmable Logic Devices: **(6 Hrs)**

Introduction, evolution: PROM, PLA, PAL, architecture of PAL's, applications, programming PLD's, FPGA with technology: antifuse, SRAM, EPROM, MUX, FPGA structures, and ASIC design flows, programmable interconnections, coarse grainedreconfigurable devices

Unit 6: IP and Prototyping: (7 Hrs)

IP in various forms: RTL source code, encrypted source code, soft IP, netlist, physical IP, and use of external hard IP during prototyping, case studies and speedissues, testing of logic circuits: fault models, BIST, JTAG interface

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- **Internal Continuous Assessment (ICA)**
  ICA shall consist of minimum 6 laboratory experiment based upon above curriculum

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- **Reference Books**

1. Douglas Smith, "HDL Chip Design: A Practical Guide for Designing, Synthesizing &Simulating ASICs & FPGAs Using VHDL or Verilog", Doone publications, 1998.
2. Samir Palnitkar, "Verilog HDL: A guide to Digital Design and Synthesis", Prentice Hall,
3. Doug Amos, Austin Lesea, Rene Richter, "FPGA based Prototyping MethodologyManual", Synopsys Press
4. Christophe Bobda, "Introduction to Reconfigurable Computing, Architectures, Algorithmsand Applications", Springer
5. Janick Bergeron, "Writing Testbenches: Functional Verification of HDL Models", SecondEdition, Springer

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-I

ADVANCED DIGITAL SIGNAL PROCESSING

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Practical –2Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Design of Digital Filters (07 Hrs)

Overview of DSP, characterization in time and frequency, FFT Algorithms, digital filter design and structures: basic FIR/IIR filter design & Structures, design techniques of linear phase FIR filters, IIR filters by Impulse invariance, bilinear transformation, FIR/IIR cascaded lattice structures.

Unit 2 :Multirate Digital Signal Processing (07 Hrs)

Multi rate DSP, decimators and interpolators, sampling rate conversion, multi tagedecimator & interpolator, poly phase filters, QMF, digital filter banks, applications in subband coding.

Unit 3: Linear Prediction & Optimum Linear Filters(07 Hrs)

Linear prediction & optimum linear filters, stationary random process, forward-backwardlinear prediction filters, solution of normal equations, AR lattice and ARMA lattice-ladder filters, Wiener Filters for filtering and prediction.

SECTION-II

Unit 4: Adaptive Filters (07 Hrs)

Adaptive filters, applications, gradient adaptive lattice, minimum mean squarecriterion, LMS algorithm, recursive least square algorithm

Unit 5: Power Spectrum Estimation (07 Hrs)

Estimation of spectra from finite-duration observations of signals, nonparametricmethods for power spectrum estimation, parametric methods for power spectrum estimation, minimum-variance spectral estimation, Eigen analysis, algorithms for spectrum estimation.

Unit 6: Wavelet Transform & Application of DSP (07 Hrs)

Application of DSP & multi rate DSP, application to radar, introduction to Wavelets,application to image processing, design of phase shifters, DSP in speech processing & other applications

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- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 laboratory experiment based upon above curriculum

- **Reference Books**

1. J.G.Proakis and D.G.Manolakis, "Digital signal processing: Principles, Algorithm and Applications", 4th Edition, Prentice Hall, 2007
2. N. J. Fliege, "Multirate Digital Signal Processing: Multirate Systems -Filter Banks – Wavelets", 1st Edition, John Wiley and Sons Ltd, 1999
3. Sanjit K Mitra ,"Digital Signal Processing-A Computer Bases Approach",3rd Edition McGraw Hill,2009
4. M. H. Hayes, "Statistical Digital Signal Processing and Modeling", John Wiley & Sons Inc., 2002
5. S.Haykin, "Adaptive Filter Theory", 4th Edition, Prentice Hall, 2001
6. D.G.Manolakis, V.K. Ingle and S.M.Kogon, "Statistical and Adaptive Signal Processing", McGraw Hill, 2000

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-I

VOICE AND DATA NETWORKS

Teaching Scheme	Examination Scheme
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Tutorial –1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION I

Unit 1-Network design issues- **(6 Hrs)**

Network design issues, network performance issues, network terminology, centralized and distributed approaches for network design, issues inn design of voice and data networks

Unit-2 Voice Networks **(6 Hrs)**

Layered and layer-less communication, cross layer communication, voice networks (wired and wireless) and switching, circuit switching and packet switching, statistical multiplexing.

Unit 3 Link layer protocols- **(8 Hrs)**

Data networks and its design, link layer design-link adaptation, link layer protocols, retransmission mechanisms-ARQ, hybrid ARQ, Go_back_N, selective repeat protocols and their analysis.

SECTION II

Unit 4- Communication across network- **(8 Hrs)**

Inter-networking, bridging, global internet, IP protocol and addressing, subnetting, classless inter domain routing (CDIR), IP address lookup, routing in internet, end to end protocols, TCP and UDP, congestion control, additive increase / multiplicative decrease. Slow start, fast retransmit / fast recovery.

Unit 5 Congestion control **(6 Hrs)**

Congestion avoidance, RED, TCP-throughput analysis, quality of service in packet networks, network calculus, packet scheduling algorithms

Unit 6 Network security- **(6 Hrs)**

Network security and management, principles of cryptography, authentication, integrity, key distribution and certification, access control and firewalls, attacks and measures

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 tutorials based upon above curriculum

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- **Reference Books**

- D. Bertsekas and R. Gallager, "Data Networks", 2nd Edition, Prentice Hall, 1992.
- L. Peterson and B. S. Davie, "Computer Networks: A Systems Approach", 5thEdition,Morgan Kaufman, 2011.
- Kumar, D. Manjunath and J. Kuri, "Communication Networking: An analyticalapproach" 1st Edition, Morgan Kaufman, 2004.
- Walrand,"Communications Network: A First Course", 2nd Edition, McGraw Hill, 2002.
- William Stalling, "Network security, essentials", Pearson education Asia publication, 4thEdition, 2011

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-I

MACHINE LEARNING

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Practical –2Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Introduction to Machi e Learning (06 Hrs.)
n

Machine learning: what and why, supervised learning, unsupervised learning, some basic concepts in machine learning, definition of learning systems, goals and applications of machine learning, aspects of developing a learning system: training data, concept representation, function approximation

(Chapter 1 from Book 1, Chapter 1 from Book 2)

Unit 2: Linear and Logistic Regression (08 Hrs)

Linear regression: introduction, model specification, maximum likelihood estimation (least squares), robust linear regression, ridge regression, Bayesian linear regression, logistic regression: introduction, model specification, model fitting, Bayesian logistic regression, online learning and stochastic optimization, generative vs discriminative classifiers.

(Chapter 7 and 8 from Book 2)

Unit 3:Decision Tree Learningand Ensemble Methods (08 Hrs)

Representing concepts as decision trees, recursive induction of decision trees, picking the best splitting attribute: entropy and information gain, searching for simple trees and computational complexity, Occam's razor, overfitting, noisy data, and pruning, ensemble methods: bagging and boosting

(Chapter 3 from Book 1, Chapter 14 from Book 3)

SECTION-II

Unit 4: Clustering (05 Hrs)

Introduction, dirichlet process mixture models, affinity propagation, spectral clustering, hierarchical clustering, dlustering data points and features

(Chapter 25 from Book 2)

Unit 5: Sparse Kernel Machines **(05 Hrs)**

Introduction to Support Vector Machines (SVM), maximum margin classifiers, relevance vector machines, applications of Support Vector Machines

(Chapter 7 from Book 3)

Unit 6: Neural Networks and Deep Learning **(08 Hrs)**

Feed-forward network functions, network training, error backpropagation, regularization in neural networks, deep learning: introduction, deep neural networks, applications of deep networks

(Chapter 5 from Book 3, Chapter 28 from Book 2)

Unit 7: Key Ideas in Machine Learning **(04 Hrs)**

Introduction, key perspectives on machine learning, key results, where machine learning is headed next

(Chapter 14 of upcoming 2nd Edition of Book 1)

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 laboratory experiment based upon above curriculum

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- **Reference Books**

1. *Book 1*: Machine Learning by Tom Mitchell, McGraw Hill (1st Edition)
2. Draft content of chapter of upcoming 2nd edition of Book 1

   http://www.cs.cmu.edu/~tom/mlbook/keyIdeas.pdf
3. *Book 2*: Machine Learning: a Probabilistic Perspective by Kevin Patrick Murphy
4. *Book 3*: Pattern Recognition and Machine Learning (Information Science and Statistics)by Christopher M. Bishop

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-I

ELECTIVE I: WIRELESS SENSOR NETWORKS

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Tutorial–1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Introduction to Wireless Sensor Networks (WSN): **(06 Hrs.)**
Motivation, overview, network architecture, protocol stack, design objectives, challenges & constraints, technologies, hardware & software platforms, standards, applications

Unit 2: Medium Access Control (MAC): **(06 Hrs.)**

Overview of MAC, MAC for WSN- network characteristics, objectives, energy efficiency, contention MAC, contention free MAC, hybrid MAC

Unit 3: Routing & Clustering: **(08Hrs)**
Overview, challenges, metrics, data centric routing, proactive routing, on demand routing, hierarchical routing, location based routing, QoS based routing, introduction to clustering

SECTION-II

Unit 4: Node Architecture: **(04 Hrs.)**
Architecture, sensing, processing, communication interface, prototypes, software subsystems

Unit 5: Power Management: **(06 Hrs.)**

Need, classification, passive power conservation mechanism, active power conservation mechanism, power control at different protocol layer

Unit 6: Time Synchronization: **(04 Hrs.)**
Clocks and synchronization problems, basics of time synchronization, time synchronization protocols

Unit 7: Localization: **(04 Hrs.)**

Ranging techniques, range based localization, range free localization, event driven localization

Unit 8: Standards **(04 Hrs)**

IEEE 802.15- Overview, MAC layer, Zigbee- network layer, application layer

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 tutorials based upon above curriculum

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- **Reference Books**

1. Wireless Sensor Networks – A Networking Perspective, Jun Zheng, Abbas Jamalipour,Wiley-IEEE
2. Fundamentals of Wireless Sensor Networks- Theory and Practice, WaltenegusDargie, ChrstianPoellabauer, Wiley
3. Networking Wireless Sensors, BhaskarKrishnamachari, Cambridge University Press
4. Wireless Sensor Networks- Technology, Protocols and Applications, KazemSohraby,Daniel Minoli, TaiebZnati, Wiley India
5. Wireless Sensor Network Designs, Anna Hac, John Wiley and Sons

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-I

ELECTIVE I: ANALOG AND DIGITAL CMOS VLSI DESIGN

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Tutorial–1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION I

Digital CMOS Design

Unit 1: Review **(7 Hrs)**

Basic MOS structure and its static behavior, quality metrics of a digital design: cost, functionality, robustness, power, and delay, stick diagram and layout, wire delay models inverter: static CMOS inverter, switching threshold and noise margin concepts and theirevaluation, dynamic behavior, power consumption.

Unit 2: Physical Design Flow: **(7 Hrs)**

Floor planning, placement, routing, CTS, power analysis and IRdrop estimation-static and dynamic, ESD protection-human body model, machine model.

*Combinational logic***:** Static CMOS design, logic effort, ratioed logic, pass transistor logic, dynamic logic, speed and power dissipation in dynamic logic, cascading dynamic gates,CMOS transmissiongate logic.

Unit 3: Sequential Logic **(8 Hrs)**

Static latches and registers, Bi-stability principle, MUX based latches,stat c SR flip-flops, master-slave edge-triggered register, dynamic latches and registers,concept of pipelining, pulse registers, non-bistable sequential circuit

Advanced technologies: giga-scale dilemma, short channel effects, hig h–k, metal gate technology, FinFET, TFET etc.

SECTION II

Analog CMOS Design:

Unit 4:Single Stage Amplifier **(8 Hrs)**

CS stage with resistance load, divide connected load, currentsource load, triode load, CS stage with source degeneration, source follower, commongatestage, cascade stage, ch ice of device models.

Differential Amplifiers: basicdifference pair, common mode response, differential pair with MOS

loads, Gilbert cell.

Unit 5: Passive and Active Current Mirrors: (6 Hrs)
Basic current mirrors, Cascade mirrors, Active currentmirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascadestage and difference pair, Noise

Unit 6: Operational Amplifiers: (7 Hrs)
One stage OPAMP, two stage OPAMP, gain boosting, commonmode feedback, slew rate, PSRR, compensation of 2 stage OPAMP, other compensationtechniques.

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 tutorials based upon above curriculum

- **Reference Books**

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
4. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
5. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
6. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",
   a. TMH, 3rdEdition.
7. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-I

ELECTIVE I: IMAGE AND VIDEO PROCESSING

Teaching Scheme	**Examination Scheme**
Lectures –3Hours/week, 3 Credits	ESE- 70 Marks
Tutorial–1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION I

Unit1: Image and Video Fundamentals :(04 Hrs.)

Image and video formats, Sampling in 2-dimension (2-D) and 3-dimension (3-D), image processing operations, digital video basics

Unit 2: Image Transforms: (06 Hrs.)

2D orthogonal & unitary transforms, discrete Fourier transform (DFT), discrete cosine transform (DCT), Hadamard transform, Haar transform, wavelet transform, Karhunen-Loeve transform (KLT), Singular value decomposition (SVD) transform.

Unit 3: Image and Video Enhancement (06 Hrs.)

Histogram, Point processing, spatial operations, transform operations, multi-spectral image enhancement, fundamentals of 2-D motion estimation and motion compensation, algorithms for

2-D motion estimation, motion-compensated filtering, frame rate conversion, deinterlacing

Unit 4: Image and Video Restoration (06 Hrs.)

Image observation models, inverse & Wiener filtering, generalized inverse, SVD and iterative methods, maximum entropy restoration, Bayesian methods, blind de-convolution, modeling in case of video restoration, intraframe shift invariant restoration, multiframe restoration

Section– II

Unit 5:Image and Video Segmentation (06 Hrs.)

Discontinuity based segmentation- line detection, edge detection, thre holding, region basedsegmentation, scene change detection, spatiotemporal change detection, motion segmentation, simultaneous motion estimation and segmentation, semantic video object segmentation

Unit 6:Image and Video Compression (06 Hrs.)

Lossless image compression including entropy coding, lossy image compression, videocompression techniques, international standards for image and video compression (JPEG, JPEG 2000, MPEG-2/4, H.264, HEVC), video quality assessment

Unit 7:Image analysis & computer vision (06 Hrs.)

Spatial feature extraction, transform features, edge detection, boundary extraction, boundary representation, region representation, moment representation, structure, shape features, texture, scene matching & detection, image segmentation, classification techniques.

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum 6 tutorials based upon above curriculum

- **Reference Books**

1. Fundamentals of Digital Image Processing, K. Jain, Pearson education(Asia) Pte. Ltd. / Prentice Hall of India, 2004
2. Handbook of Image & Video Processing, Al Bovik, Elsevier Academic Press, 2nd Edition
3. Multidimensional Signal, Image and Video Processing and Coding, John W. Woods, Academic Press, Elsevier, 2006.
4. Fundamentals of Multimedia, Z. Li, M.S. Drew,Pearson education (Asia) Pte. Ltd., 2004
5. Digital Image Processing,R. C. Gonzalez, R. E. Woods, Pearson education (Asia) Pte. Ltd. /Prentice Hall of India, 2004, 2nd Edition
6. Digital Video Processing, M. Tekalp,Prentice Hall, USA, 1995

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-II

RESEARCH METHODOLOGY& IPR

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Tutorial –1 Hour/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Research fundamentals: (6 Hrs.)

Definition, objectives, motivation, types of research and approaches, research- descriptive, conceptual, theoretical, applied and experimental

Unit 2: The initial research process: (6 Hrs.)

Literature review, research design, assortment of the problem, identification of problem, defining a problem, objective, sub objective and scope, assumptions, validation criteria, research proposal(synopsis)

Unit 3: Report writing and presentation of results: (5 Hrs.)

Need, report structure, formulation, sections, protocols, graphs, tables, IEEE format, evaluation of report, writing abstract, writing technical paper

Unit 4: Information communication technology: (3 Hrs.)

Introduction, e-research, indices, virtual lab, digital lab, ethical issues in research

SECTION-II

Unit 5: Mathematical modeling and simulation: (7 Hrs.)

Mathematical modeling – need, techniques and classification, system models –types, static, dynamic, system simulation – why to simulate, technique of simulation, Monte Carlo simulation, types, continuous modeling, discrete model, role of probability and statistics in simulation, statistical distributions,

Unit 6: Nature of Intellectual Property: (7 Hrs.)

Patents, designs, trade and copyright, process of patenting and development: technological research, innovation, patenting, development, international scenario: international cooperation on intellectual property, procedure for grants of patents, patenting under PCT.

Unit 7: Patent Rights: **(6 Hrs.)**

Scope of patent rights, licensing and transfer of technology, patent information and databases, geographical indications

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- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum seven assignments based upon above syllabus

- **Reference Books**

1. Fundamental of Research Methodology and Statistics, Yogesh Kumar Sing, New Age International Publishers
2. Research Methodology: Methods and Techniques, C.R. Kothari, New Age International Publishers, 2nd revised Edition
3. Research Methodology, Concepts and Cases, Deepak Chawla, NeenaSondhi, Vikas
4. Intellectual Propertyin New Technological Age, Robert P. Merges, Peter S. Menell, Mark A. Lemley, 2016.
5. Intellectual Property Rights by Neeraj Pandey And Khushdeep Dharn
6. Intellectual Property Rights Under WTO,T. Ramappa, S. Chand, 2008
7. Intellectual Property Rights Journal by CSIR-National institute of science Communication and Information Resources. (*January 2017 and March-May-2018*)

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M. Tech. (Electronics) Semester-II

COMMUNICATION BUSES AND INTERFACES

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Practical-2 Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Bus Systems **(5 Hrs)**
Serial Buses, physical interface, data and control signals, features.

Unit 2: Serial interfaces- **(8 Hrs)**
RS232, RS485, I^2C, SPI with their limitations and applications.

Unit 3: CAN in automation- (**7 Hrs**)
CAN - architecture, data transmission, layers, frame formats, applications

SECTION-II

Unit 4: Peripheral component interconnect- **(8 Hrs)**
PCI, PCIexpress - revisions, configuration space, hardware protocols and applications

Unit 5:Universal serial bus- **(6 Hrs)**
Transfer types, enumeration, descriptor types and contents, device driver

Unit 6:Data transfer- **(6 Hrs)**
Data streaming serial communication protocol- serial front panel data port (SFPDP) using fiber optic and copper cable

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 laboratory experiments based upon above curriculum

- **Reference Books**

1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ”, Lakeview Research, 2nd Edition
2. Jan Axelson, “USB Complete”, Penram Publications
3. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press
4. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x
6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M. Tech. (Electronics) Semester-II

ADVANCED INTERNET OF THINGS

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Practical –2 Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION- I

Unit 1: Introduction to IoT **(7 Hrs.)**

Smart cities and IoT revolution, Fractal cities, From IT to IoT, M2M and peer networking concepts, Ipv4 and IPV6

Unit 2:**Communication Protocols** **(7 Hrs.)**

Software defined networks SDN, from cloud to fog and MIST net working for IoT communications, principles of edge/P2P networking, protocols to support IoT communications, modular design and abstraction, security and privacy in fog.

Unit 3: **Wireless Sensor Networks** **(6 Hrs.)**

Introduction, IOT networks (PAN, LAN and WAN), edge resource pooling and caching, client side control and configuration

SECTION II

Unit 4: IoT Platforms. **(7 Hrs.)**

Smart objects as building blocks for IoT, open source hardware and embedded systems platforms for IoT, edge/gateway, IO drivers, C Programming, multithreading concepts

Unit 5:IoT Operating Systems **(7 Hrs.)**

Operating systems requirement of IoT environment, study of mbed, RIoT, and Contiki operating systems, introductory concepts of big data for IoT applications

Unit 6: Applications of IoT **(6 Hrs.)**

Connected cars IoT transportation, smart grid and healthcare sectors using IoT, security and legal considerations

- **Internal Continuous Assessment (ICA)**
  ICA shall consist of minimum 6 laboratory experiment based upon above curriculum.

- **Reference Books**

1. A Bahaga, V. Madisetti, “Internet of Things- Hands on approach”, VPT publisher, 2014.
2. The Internet of Things: Enabling Technologies, Platforms, and Use Cases", by PethuruRaj and Anupama C. Raman (CRC Press)
3. Industry 4.0: The Industrial Internet of Things”, by Alasdair Gilchrist (Apress)
4. A. McEwen, H. Cassimally, “Designing the Internet of Things”, Wiley, 2013.
5. CunoPfister, “Getting started with Internet of Things”, Maker Media, 1st edition, 2011.
6. Samuel Greenguard, “Internet of things”, MIT Press, 2015.

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-II

PLC, SCADA AND DISTRIBUTED CONTROL SYSTEMS

Teaching Scheme	Examination Scheme
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Practical –2 Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: Automation fundamentals **(7 Hrs)**

Automation and its importance, automation applications, expectations of automation, process and factory automation. Types of plant and control- categories in industry, open loop and closed loop control functions, continuous, discrete and mixed processes, automation hierarchy – large control systems, data quantity, quality and hierarchical control. Control system architecture – evolution and current trends, comparison of different architectures

Unit 2:Programmable Logic Controller Hardware **(7 Hrs)**

Evolution of PLC, definition, functions of PLC, advantages and architecture, working of PLC, scan time, types & specifications, digital input, digital output, analog input, analog output examples and ratings, I/O modules, local and remote I/O expansion, communication modules & special purpose modules, memory and addressing – memory organization (system memory & application memory), I/O addressing, hardware to software interface.

Unit 3: PLC Programming **(7 Hrs)**

Software development of relay logic Ladder diagram, introduction to PLC programming, programming devices, IEC standard PLC programming languages, ladder diagram programming: basic instructions, PLC timers and counters: types and examples, data transfer & program control

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instructions, advanced PLC instructions, PID control using PLC. Case study: PLC selection and configuration for any one process applications.

SECTION-II

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Unit 4:Distributed control System (DCS) **(7 Hrs)**

Introduction to DCS, evolution of DCS, DCS flow sheet symbols, architecture of DCS, controller, input and output modules, communication module, data highway, local I/O bus, workstations, specifications of DCS, DCS system integration with PLCs: HMI, man machine interface sequencing, supervisory control and integration with PLC, personal computers and direct I/O, serial linkages, network linkages, introduction to DCS programming, function block diagram method for DCS programming.

Unit 5:Supervisory Control and Data Acquisition Systems (SCADA) (7 Hrs)
SCADA: Introduction, brief history, elements of SCADA, features of SCADA, MTU- functions of MTU, RTU- functions of RTU, protocol details of SCADA- types and methods used, components, protocol structures and mediums used for communications, SCADA development for any one typical application, programming for GUI development using SCADA software.

Unit 6: Applications of PLC and SCADA (7 Hrs)
Systems block diagram, operation, ladder diagram and explanation for following applications: steam boiler control system using PLC, conveyer belt automation system, automation of bottle filling plant, material flow measurement systems and traffic light controller using PLC.

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum 6 laboratory experiments based upon above curriculum

- **Reference Books**

1. John. W. Webb & Ronald A. Reis, "Programmable Logic Controllers- Principles and Applications", PHI , 5th Edition, 2002
2. Frank D. Petruzella, "Programmable Logic Controllers", Mc Graw Hill Education, 4th Edition, 2016
3. Gary Dunning, "Introduction to Programmable Logic Controllers", Thomson Learning, Pck Edition 2001
4. Stuart Boyer, " SCADA : Supervisory Control And Data Acquisition", International Society of Automation publication, 4th Edition, 2009
5. Samuel M. Herb, "Understanding Distributed Processor Systems For Control", International Society of Automation Publication, 1st Edition 1999
6. Krishna Kant, "Computer Based Process control", PHI 2nd Edition 2010

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-II

ELECTIVE II- MOBILE TECHNOLOGY

Teaching Scheme	**Examination Scheme**
Lectures –3 Hours/week, 3 Credits	ESE- 70 Marks
Tutorial –1 Hours/week, 1 Credit	ISE- 30 Marks
	ICA – 25Marks

SECTION-I

Unit 1: GSM System Overview: (8 Hrs)

GSM architecture, location tracking and call set up, security, data services, network signaling, MAP protocol and dialogue, mobility management, databases, failure rest ration, overflow o control, SMS protocol, international roaming, operations, administration and maintenance

Unit 2: General Packet Radio Services (GPRS): (6 Hrs.)

Functional groups, architecture, network nodes, interfaces, procedures, billing, mobility management, applications, EDGE

Unit 3: Wireless Application Protocol (WAP): (6 Hrs.)

Model, gateway, protocol, user agent profile and caching, wireless bearers, development toolkit, network and application environments, wireless markup language, telephony applications, MMS, other applications

SECTION II

Unit 4: Universal Mobile Telecommunication Services (UMTS): (7 Hrs.)

Migration path, air interfaces, URRAN architecture, speech call, packet data, handover, core network evaluation

Unit 5: CDMA 2000: (7 Hrs.)

Evaluation, network architecture and structure, radio network, 1xEVDO, 1xRTT

Unit 6: Security Issues in Mobile Technology: (6 Hrs.)

Information security, attacks, components of information security, security techniques and algorithms, security protocols, security models and frameworks

- **Internal Continuous Assessment (ICA)**

  ICA consist of minimum six assignments based upon above syllabus

- **Reference Books**

1. Mobile Computing, Technology, applications and Service Creation, Asoke K. Talukder, Hasan Ahmed, Rupa R. Yavagal, Tata McGraw Hill Education Pvt. Ltd.,2nd Edition
2. 3G Wireless Networks, Clint Smith, Daniel Collins, Tata McGraw Hill Publishing Company Ltd., 2nd Edition
3. Wireless and Mobile Network Architecture, Yi-Bing Lin, Imrich Chlamtac, Wiley India

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics Engineering) Semester-II

ELECTIVE-II: REAL TIME SYSTEMS

Teaching Scheme
Lectures: 3 hrs/week, 3 Credits
Tutorial: 1 hr /week, 1 Credit

Examination Scheme
ESE –70 Marks
ISE – 30 Marks
ICA- 25 Marks

SECTION I

Unit 1: Introduction **(7 Hrs)**

Introduction , issues in real time computing , structure & application of a real time system , task classes ,performance measures for real time systems, estimating program run times, task assignment and scheduling, classical uniprocessor scheduling algorith s, uniprocessor m
scheduling of iris tasks, task assignment ,modelling timing constraints

Unit 2:Programming Languages and Tools- I **(7 Hrs)**

Programming languages and tools, desired language characteristics, data t y ping, control & conditional structures, facilitating hierarchical decomposition, packages

Unit 3: Programming Langua es and Tools -II **(7 Hrs)**
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Run time (exception) error handling, overloading and generics, multitasking, low level programming, task scheduling, timing specifications, programming environments, run time support

SECTIONB II

Unit 4: Real Time Databases **(7 Hrs)**

Real time databases ,basic definition, real time vs general purpose databases, main memory databases, temporal data, transaction priorities, transaction aborts, concurrency control issues, disk scheduling algorithms, two phase approach to improve predictability , serialization consistency , databases for hard real time systems.

Unit 5:Real –Time Communication **(7 Hrs)**

Real time communication, communications media, network topologies protocols, fault tolerant routing, fault tolerance techniques, fault types, fault detection, fault error containment redundancy, data diversity, reversal checks, integrated failure handling.

Unit 6: Evaluation techniques **(7 Hrs)**

Reliability evaluation techniques, obtaining parameter values, reliability models for hardware redundancy, software error models, clock synchronization, clock, an on fault, tolerant synchronization algorithm, impact of faults, fault tolerant synchronization in hardware, fault tolerant synchronization in software.

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum six assignments based upon above syllabus

- **Reference Books**

1. C.M. Krishna, Kang G. Shin, "Real – Time Systems", McGraw – Hill International Editions, 1997.
2. Rajib Mall, "Real-time systems: theory and practice", Pearson Education, 2007
3. S. T. Allworth and R. N. Zobel, " Introduction to real time software design", McMillan, 2nd Edition, 1987
4. R.J.A Buhur, D.L Bailey, "An Introduction to Real – Time Systems", Prentice – Hall International, 1999.

Philip.A.Laplante, "Real Time System Design and Analysis", Prentice Hall of India, 3rd

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech (Electronics) Semester-II

ELECTIVE II-VLSI IN SIGNAL PROCESSING

Teaching Scheme	**Examination Scheme**
Lectures: 3 hrs/week, 3 Credits	ESE –70 Marks
Tutorial: 1 hrs/week, 1 Credit	ISE – 30 Marks
	ICA- 25 Marks

SECTION- I

Unit1: DFG Representation and Iteration Bound (6 Hrs)

Representations of DSP algorit ms, data flow graph representations, critical path, loop bound, h
iteration bound, algorithms for computing iteration bound

Unit2: Pipelining and Parallel Processing (6 Hrs.)

Pipelining approach to reduce critical path, parallel processing to handle higher sample rates, power reduction computations, combined pipelining and parallel processing

Unit 3: Retiming (8 Hrs.)

Introduction to retiming, definitions and properties, solving system of inequalities, cut set retiming and pipelining, retiming for clock period minimization, retiming for register minimization

SECTION II

Unit 4:Unfolding (6 Hrs.)

Introduction to unfolding, algorithm for unfolding, properties of unfolding, applications of unfolding

Unit 5:Folding (5 Hrs.)

Introduction to folding, folding transformation, lifetime analysis for register minimization in folded architecture

Unit 6:Systolic Array Design (5 Hrs.)

Methodologies, family of systolic arrays (FIR filter) using linear mapping techniques, matrix – matrix multiplication

Unit 7:Bit Level Arithmetic Architectures (4 Hrs.)

Parallel multiplication with sign extension**,** parallel carry ripple array multipliers, parallel carry save array multipliers, parallel multipliers with modified booth recording

- **Internal Continuous Assessment (ICA)**

  ICA shall consist of minimum seven assignments based upon above syllabus

- **Reference Books:**

1. VLSI Digital Signal Processing Systems- Design and Implementation, Keshav K. Parhi, Wiely (India)
2. Architecture for Digital Signal Processing, Peter Pirsch, Wiley India
3. Digital Signal Processing in VLSI,Richard J. Higgins
4. VLSI Synthesis of DSP Kernels-Algorithmic and Architectural Transformations, Mahesh Mehendale, Sunil D. Sherlekar

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-III

Self Learning Course

NETWORK AND INTERNET SECURITY

Examination Scheme
Theory Credits – 3.0

SECTION-I

Unit 1: Introduction:
Overview of ISO's OSI model and TCP/IP model, key management, public-key infrastructure (PKI), remote user authentication using symmetric key encryption, Kerberos, remote user authentication using asymmetric key encryption, federated identity management, biometrics

Unit 2: Wireless network security:
IEEE 802.11 wireless LAN overview: IEEE 802.11 network components, architectural model, IEEE 802.11 services; IEEE 802.11i wireless LAN security: IEEE 802.11i services, IEEE 802.11i phases of operation, discovery phase, authentication phase, key management phase & protected data transfer phase, IEEE 802.11i pseudorandom function

Unit 3: WAP security:
Wireless application protocol (WAP): WAP architecture, wireless application environment, WAP protocol architecture; wireless transport layer security (WTLS): WTLS sessions and connections, WTLS protocol architecture, cryptographic algorithms**,** WAP end-to-end security

SECTION II

Unit 4: Electronic mail security:
Pretty good privacy (PGP): notation, operational description, cryptographic keys and key rings, public-key management, S/MIME: RFC 5322, multipurpose internet mail extensions, S/MIME functionality, S/MIME messages, S/MIME certificate processing, enhanced security services, domain keys identified mail**:** internet mail architecture, e-mail threats, DKIM strategy, DKIM functional flow

Unit 5: Web and IP security:
Web security: web security requirements, secure sockets layer (SSL), transport layer security (TLS), and secure electronic transaction (SET), HTTPS, secure shell (SSH), IP security: IP security overview, architecture, authentication, encapsulating security payload, combining security associations, key management

Unit 6: System security:
Intruders, intrusion detection; password management, malicious software, viruses and related threats, virus countermeasures, distributed denial of service attacks, firewalls: firewall design, principles, trusted systems

- **Text Books:**
  1. Cryptography and Network Security: Principles and Practice, 5th Edition, William Stallings, Pearson Education, ISBN: 978-81-317-6166-3
  2. Cryptography and Network Security, Behrouz A. Forouzan, Tata McGraw-Hill. 2007, ISBN: 978-00-706-6046-5

- **Reference Books:**
  1. Network Security And Cryptography, Bernard Menezes, Cengage Learning, 2010, ISBN : 978-81-315-1349
  2. Applied Cryptography, 2nd Edition, Schneier B, Wiley & Sons. 2002, ISBN: 0-471-11709-9

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-IIISelf Learning Course

PROGRMMABLE SYSTEM ON CHIP (PSoC)

Examination Scheme
Theory Credits – 3.0

SECTION-I

Unit 1: Introduction to PSoC:
PSoC technology, programmable routing and interconnect, configurable analog and digital blocks, cpu sub system, families of PSoC (PSoC 1, PSoC 3, PSoC 5), difference between PSoC and conventional MCU.

Unit 2: Introduction to PSoC 3/5:
PSoC 3/5, architecture – block diagram, system wide resources, I/O interfaces, CPU sub system, memory organization, digital sub systems, analog sub systems

Unit 3: PSoC design modules:
Why cypress PSoC, structure of PSoC, PSoC designer suit, limitations of PSoC, improvements of the PSoC, PSoC sub system design, PSoC memory management.

SECTION-II

Unit 4: Mixed-signal embedded design:
Overview of mixed-signal embedded system designs, hardware and software subsystems of mixed-signal architecture, PSoC hardware components, PSoC software components, PSoC interrupt sub system, introduction to PSoC express, system design using PSoC express.

Unit 5: PSoC components:
Universal digital blocks (UDB), UDB arrays and digital system interconnect (DSI), timer, counter and PWM, digital filter blocks (DFB), $\Delta\sum$ ADC topologies and circuits, programmable gain amplifiers, switched capacitor / continuous time, analog routing, flash temperature sensors, DTMF dialers, sleep timers, UART, I2 C, SPI, USB, CAN buses.

Unit 6: System design using PSoC:
Interfacing of temperature sensors and tachometers, SPI and UART based task communications, lower noise continuous time signal processing with PSoC, data acquisition and control system with PSoC, ultra wide-based RADAR, serial bit receiver with hardware Manchester decoder, DTMF detector, ultrasonic vehicle parking assistant, universal wide-range signal generator.

- **Text Books:**

1. PSoC 3, PSoC 5 Architecture technical reference manual, Cypress website
2. My First Five PSoC 3 design (e-book), Robert Asbhby, Cypress website

- **Reference Books:**

1. Designer Guide to the Cypress PSoC, Robort Ashby, Elsevier Publications
2. Introduction to Mixed Signal Embedded Design, Alex Doboli, Springer
3. The Beginners Guide to Using PSoC Express: Mixed-Signal Microcontroller Development without Code, Oliver H. Bailey, Timelines Industries Incorporated, 2007
4. PSoC Mikrocontroller by Fredi Kruger Franzis, 2006

- **Web References:**

1. www.cypress.com/go/psoc
2. www.cypress.com/go/trainning
3. www.cypress.com/go/support
4. www.psocdeveloper.com

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-III Self Learning Course

ADVANCED PROCESS CONTROL

Examination Scheme
Theory Credits – 3.0

SECTION-I

Unit 1: Process dynamics and mathematical modeling:
Modeling procedure, linearization, numerical solutions of ordinary differential equations, input-output models and transfer functions, dynamic behavior of typical process systems, serial & parallel structures of simple systems, multiple input-multiple output systems

Unit 2: Empirical model identification:
An empirical model building procedure, process reaction curve methods, statistical model identification.

Unit 3: Conventional feedback control system:
Desired features of a PID controller, PID controller tuning for dynamic performance, stability analysis of control systems, controller tuning based on stability: Ziegler – Nichols closed loop method, digital implementation of process control, effects of digital control on stability, tuning and performance, performance of feedback control systems

Unit 4: Cascade & feed forward control:
Cascade control: design criterion, cascade performance, controller algorithm & tuning, implementation issues; feed forward control: design criterion, feed forward performance, controller algorithm and tuning, implementation issues; analyzing a nonlinear process with linear feedback control, different issues in improving nonlinear process performance

SECTION-II

Unit 5: Model based control:
The structure of model based control, modeling approaches, internal model control (IMC),the Smith predictor, model predictive control (MPC), process model based control (PMBC), implementation guidelines.

Unit 6: Nonlinear adaptive control:
Adaptation of feedback parameters, programmed adaptation, switching controller gains and self-tuning controllers: model based methods, model reference adaptive control, pattern recognition controllers.

Unit 7: Multivariable control:
Multi-loop control, effects of interaction, performance analysis, multivariable predictive control and dynamic matrix control (DMC) approach for signal variable and multivariable, implementation issues in DMC.

Unit 8: Statistical process control:

Shewhart chart, interpretation of chart, distinction between automatic process control (APC) & statistical process control (SPC), implementing SPC concepts.

- **Reference Books:**
  1. Process Control: Designing Processes & Control Systems for Dynamic Performance, Thomas E.Marlin, McGRAW Hill International Edition.
  2. Process Control: Instrument Engineers Handbook, Editor, Bela G. Liptak, Butterworth - Heinemann Publishers.
  3. Process Dynamics: Modeling, Analysis & Simulation, B. Wayne Bequette, Prentice Hall International Edition.
  4. Process Modeling, Simulation and Control for Chemical Engineers, William Luben, McGraw Hill International Edition.
  5. Process control systems: Application, Design and Turning, F.G. Sinskey, McGraw Hill Publication Applied Process Control by

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-III

Open Elective Course

BUSINESS ANALYTICS

Teaching Scheme
Lectures –3 Hours/week, 3 Credits

Examination Scheme
ESE- 70 Marks
ISE- 30 Marks

SECTION-I

Unit 1: Introduction **(4 Hrs)**

What Is Business Analytics? Business Analytics Process, Relation of BA process and Organization decision making process

What is Data Mining? Data Mining and Related Terms, Big Data, Data Science, Terminology and Notation in Data mining

Unit 2: Overview of the Data Mining Process **(5 Hrs)**

Core Ideas in Data Mining, Classification, Prediction, Association Rules and Recommendation Systems, Predictive Analytics, Data Reduction and Dimension Reduction, Data Exploration and Visualization, Supervised and Unsupervised Learning, Steps in Data Mining, Organization of Data sets

Unit 3: Data Visualization **(5 Hrs)**

Uses of Data Visualization, Basic Charts: Bar Charts, Line Graphs, and Scatter Plots, Distribution Plots: Box plots and Histograms, Heat maps: Visualizing Correlations and Missing Values

Multidimensional Visualization: Adding Variables: Color, Size, Shape, Multiple Panels, and Animation

Manipulations: Rescaling, Aggregation and Hierarchies, Zooming, Filtering, Reference: Trend Lines and Labels, Scaling up to Large Datasets

Unit 4: Dimension Reduction **(4 Hrs)**

Introduction, Curse of Dimensionality, Data Summaries, Summary Statistics, Aggregation and Pivot Tables, Correlation Analysis, Reducing the Number of Categories in Categorical Variables, Converting a Categorical Variable to a Numerical Variable, Principal Components Analysis

SECTION-II

Unit 5: Performance Evaluation **(5 Hrs)**

Evaluating Predictive Performance, Naive Benchmark: The Average, Prediction Accuracy Measures Comparing Training and Validation Performance, Lift Chart, Judging Classifier Performance, Benchmark: The Naive Rule, Class Separation, The Confusion (Classification) Matrix, Using the Validation Data, Accuracy Measures

Unit 6: Multiple Linear Regression **(4 Hrs)**

Explanatory vs. Predictive Modeling, Estimating the Regression Equation and Prediction, Variable Selection in Linear Regression, Reducing the Number of Predictors

Unit 7: Classification & Regression Trees **(5 Hrs)**

Introduction, Classification Trees, Recursive Partitioning, Measures of Impurity, Tree Structure, Classifying a New Record, Evaluating the Performance of a Classification Tree, Navie Bayes Classifier

Regression Trees : Prediction, Measuring Impurity, Evaluating Performance

Advantages and Weaknesses of a Tree

Unit 8: Clustering **(4 Hrs)**

Introduction, Feature selection for clustering: Filter models and Wrapper models, k-Means algorithm

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- **In Semester Evaluation (ISE)**

  ISE shall be based upon minimum 6 assignments based on curriculum and consisting of literature survey, case study, data compilation and analysis etc.

- **Text and Reference Books**

1. Data Mining for Business Analytics - Concepts, Techniques, And Applications In R, Galit Shmueli Peter C. Bruce Inbal Yahav Nitin R. Patel Kenneth C. Lichtendahl, Jr., Wiley Publication *https://edu.kpfu.ru/pluginfile.php/274079/mod_resource/content/2/DatMiningBusAnalytics.pdf*
2. Data Science and Big Data Analytics: Discovering, Analyzing, Visualizing and Presenting Data by EMC Education Services (2015)
3. Business Analytics – Principles, Concepts and Applications, Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson Education Limited
4. Data Mining : The Textbook, Charu C. Agrawal, Springer Publications

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-III

Open Elective Course

OPERATION RESERACH

Teaching Scheme
Lectures –3 Hours/week, 3 Credits

Examination Scheme
ESE- 70 Marks
ISE- 30 Marks

SECTION-I

Unit 1: **(5 Hrs)**
OR Models, model formulation, Linear Programming models, Graphical solution, Simplex techniques, Two Phase method

Unit 2: Duality theory - Properties of Primal and Dual Optimal Solutions, Duality Simplex method , Shadow Price- Sensitivity analysis **(5 Hrs)**

Unit 3: Simulation Techniques - Need of Simulation techniques , Monto-Carlo Simulation, random number concept, applications of Simulation technique **(5 Hrs.)**

Unit 4: Queuing Models - Introduction, Structure of queuing system, Terminology (Kendal's Notations) and Applications. Queuing Model M/M/1: /FIFO, **(3 Hrs.)**

SECTION II

Unit 5 : Inventory control - Inventory costs, Economic order quantity, deterministic models with or without shortages - probabilistic models - Price break model, Selective Inventory management techniques. **(5 Hrs.)**

Unit 6: Replacement analysis - Replacement models - Replacement policy for items considering change in money value with time - Individual replacement policy - Group replacement policy **(5 Hrs.)**

Unit 7: Network flow models - Minimal Spanning Tree problems -Shortest route probems - Dijiktra's algorithm - Maximal Flow problem **(3 Hrs.)**

Unit 8 : PERT and CPM Networks - floats and applications - Network crashing - Cost optimization - Resource allocation and scheduling **(5 Hrs.)**

- **In Semester Evaluation (ISE)**
  ISE shall be based upon minimum 5 assignments and at least one case study.

- **Reference Books**

  1. Operations Research by Hillier and Lieberman TMGH
  2. HamdyTaha, “Operations Research – An Introduction”, 7th edition PHI (2003)
  3. S. D. Sharma, “Operation Research”, Kedarnath and Rannalt Pub.
  4. Hira and Gupta, “Operation Research”, S. Chand and Co.
  5. N. D. Vohra, “Quantitative Techniques in Management”, TMGH
  6. Shrinath L.S.: PERT & CPM –Affiliate East West Press
  7. Anand Sharma " Quantitative Techniques for decision making" Himalaya publishing house
  8. Billy E. Gillet - " Introduction to Operations Research" TMGH
  9. R.Panneerselvan " Operations Research" PHI

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-

IIIOpen Elective Course

COST MANAGEMENT OF ENGINEERING PROJECTS

Teaching Scheme
Lectures –3 Hours/week, 3 Credits

Examination Scheme
ESE- 70 Marks
ISE- 30 Marks

SECTION I

Unit 1: Cost and Cost Analysis **(8 hours)**

Cost:- Cost Elements - Pricing , Materials ,Labor , Engineering , Equipment, Parts and Tools; Economic Costs ;

Cost Analysis:- Diect Cost, indirect Cost, Overhead, allowance, Contingency

Unit 2: **Cost Estimating:** **(7 hours)**

Estimating Models; Parametric estimating- moduler estimating, parametric model , Analogous estimating- ratio estimating, The Three-quarters rule, The Square root rule, Two-Thirds rule, Range estimating

Unit 3: Progress & Cost Control: **(7 hours)**

Progress Measurement and Earned Values; Earned Value for Variable Budgets; Tracking Cost and Schedule Performance;

SECTION II

Unit 4: Cost Management: **(8 hours)**

Causes of Change, Feed Forward Techniques, Impact of schedule on cost, Lifecycle costs, Impact of project risk, integrated cost management programme.

Unit 5: Value Management: **(7 hours)**

Concept of Value ,Dimensions and Measures of Value , Overview of Value Management, Definition' Scope, Key Principles of VM , Key Attributes of VM ,Value Management Terms , Need for Value Management in Projects , The Value Management Approach ,Cross-functional Framework ' Use of Functions, Structured Decision Process, The VM Process, Benefits of Value Management, Other VM requirements

Relationship between Project Value and Risk, Value Management as an Aid to Risk Assessment

Unit 6: Value Analysis: **(7 hours)**

Earned Value Management for assessing project performance, Earned Value Management, Earned Value Management Model, Fundamentals of Earned Value, EVM Terminology, Relevancy of Earned Value Management, Conducting an Earned Value Analysis, Performing an Earned Value Assessment, Managing a Portfolio of Projects with Earned Value Management, Important Issues in the Effective Use of Earned Value Management

Integrating Cost and Value in Projects.

- **In Semester Evaluation (ISE)**

  ISE shall be based upon minimum 6 assignments based on curriculum and consisting of literature survey, case study, data compilation and analysis etc

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- **Text and Reference Book:-**

1. Project Estimating and Cost Management By Parivs F. Rad PhD, PMP
2. Project Cost Management guide from PMBOK 5th edition
3. Project Scheduling and Cost Control: Planning, Monitoring and Controlling the Baseline by James Taylor
4. Systems Life Cycle Costing: Economic Analysis, Estimation, and Management, John V. Farr, Draft Textbook, Version 1.0.
5. COST AND VALUE MANAGEMENT IN PROJECTS Ray R. Venkataraman and Jeffrey K. Pinto John Wiley & Sons, Inc Inc., Hoboken, New Jersey
6. American Association of Cost Engineers, "SKILLS AND KNOWLEDGE OF COST ENGINEERING", 1996
7. Cost Management of Capital Projects (Cost Engineering) by Kurt Heinze – International Edition, August 28, 1996

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-

IIIOpen Elective Course

PRODUCT DESIGN AND DEVELOPEMNT

Teaching Scheme
Lectures –3 Hours/week, 3 Credits

Examination Scheme
ESE- 70 Marks
ISE- 30 Marks

SECTION I

Unit 1: Introduction to product design and development **(6 hours)**

Product life cycle, Product policy of an organization and profitable product selection, Product design, Product design steps and analysis

Unit 2 **Value Engineering and analysis:** **(6 hours)**

Value Engineering concepts, Problem Identification, Functional analysis Functional analysis system steps, Case study on Value Engineering and analysis

Unit 3: Quality Function Deployment : **(7 hours)**

Computer Aided Design, Robust Design, Design for X Ergonomics in product design

SECTION II

Unit 4: Ergonomics in product design: **(8 hours)**

Ergonomics/ Human factors, Posture and movement, Ergonomic design process, Performance support and design intervention, Design Ergonomics in India: scope for exploration

Unit 5: DFMA (Design for Manufacturing and Assembly): **(7 hours)**

DFMA guidelines, Product Design for manual assembly, Design guidelines for different processes, Rapid prototyping – concepts and advantages, Prototyping processes.

Unit 6: Economic Decision: **(7 hours)**

Making/Cost Evaluation, Life cycle analysis Planning and Scheduling, Planning for manufacturing, Project planning, Risk and Opportunity Management, Metrics for Design and Development Program, Leadership Management and Control, Project start-up, Plans/schedules Design for Cost: Design for Six Sigma: Process, Invent, Innovate, Develop, Optimize and Verify.

- **In Semester Evaluation (ISE)**
  ISE shall be based upon minimum 6 assignments based on curriculum.

- **Text and Reference Book :-**

1. Ulrich, Karl, and Steven Eppinger. Product Design and Development. McGraw-Hill,

2. Kemnneth Crow: Concurrent Engg./Integrated Product Development, DRM

3. Staurt Pugh: Tool Design -Integrated Methods for Successful Product Engineering, Addison Wesley Publishing, New York, NY

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M. Tech. (Electronics) Semester-III

Dissertation Phase I: Synopsis Submission Seminar

Examination Assessment Scheme

Credits: 3 **ICA – 100 Marks**

- The student is expected to carry out intensive literature survey for a period of about two months in the field of interest and to select a topic for his/her dissertation in consultation with the faculty advisor assigned.
- The student shall then submit a report and deliver a seminar on the problem chosen by him/her to the panel of three departmental PG recognized faculty members.
- It is expected that a student justifies the gravity and also the relevance of the problem through his/her seminar. This shall be for the approval of synopsis.
- The assessment of Synopsis Submission Seminar shall be done by aforesaid panel of three departmental PG recognized faculty members.

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-III

Dissertation Phase II : ICA

Examination Assessment Scheme

Credits: 3 **ICA – 100 Marks**

- Student shall submit a report to the faculty advisor, on the basis of work carried out in accordance with instructions given by faculty advisor, throughout the semester. Dissertation Phase II evaluation consists of term-work evaluation (ISE) based on the efforts put in by the student to carry out his/her work & the results obtained.
- The faculty advisor shall complete the assessment of the report and accordingly allocate the marks to the student out of maximum 100 marks.

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M.Tech. (Electronics) Semester-III

Dissertation Phase II : Progress Seminar

Examination Assessment Scheme

Credits: 3 **ICA – 100 Marks**

- Progress seminar shall be delivered capturing details of the work done by the student for dissertation. Student shall deliver seminar using modern presentation tools.
- A hard copy of report shall be submitted to the faculty advisor before delivering the seminar. A PDF copy of the report must be submitted to the faculty advisor along with other details if any.
- End Semester Evaluation (ESE) shall consist of presentation of progress seminar on the report submitted by the student, followed by demonstration before a panel of three departmental PG recognized faculty members.

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M. Tech. (Electronics) Semester-IV

Dissertation Phase III – Progress Seminar

Examination Assessment Scheme

Credits: 3 **ICA – 200 Marks**

- For all activities related to Phase III, student must interact regularly every week with the faculty advisor. The student who has cleared his/her Phase II evaluation, shall submit a report and present the status of work carried out on the dissertation after 8-10 weeks of Phase II ESE to three departmental PG recognized faculty members.
- Progress seminar shall be delivered capturing details of the work done by student for dissertation. Student shall deliver seminar using modern presentation tools.
- A hard copy of report shall be submitted to the faculty advisor before delivering the seminar. A PDF copy of the report must be submitted to the faculty advisor along with other details if any. The evaluation will be done by the aforesaid panel of three departmental PG recognized faculty members based on the requirements of completion of dissertation work for the dissertation Phase III.

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M. Tech. (Electronics) Semester-IV

Dissertation Phase IV

Examination Assessment Scheme

Credits: 3 **ICA – 200 Marks**

- After completing the dissertation work to the satisfaction of faculty advisor, the student shall submit the dissertation report to the University in the prescribed format.
- The final approved dissertation shall be submitted in black bound hard copy. The evaluation of dissertation is to be carried out by the faculty advisor as ICA. This evaluation shall be on the basis of the requirements of completion of dissertation work.
- The faculty advisor shall submit mark list of term work marks, along with the submission of dissertation to university as mentioned in assessment scheme.

PUNYASHLOK AHILYADEVI HOLKAR SOLAPUR UNIVERSITY, SOLAPUR

M. Tech. (Electronics) Semester-IV

Final Submission of the Dissertation and Viva –Voce

Examination Assessment Scheme

Credits: 3 **ICA – 200 Marks**

- Open defense of the student on his/her dissertation shall be arranged by the university.
- This defense shall be in front of the panel of examiners as appointed by university authority. The evaluation will be done by panel of examiners as appointed by university authority.